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Study of The Temperature Dependence Model Parameters on NMOSFET in BSIM3V3

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Abstract

This article describes the study of the temperature dependence model parameters on NMOSFET in BSIM3V3. The testing MOSFET at the size of *W/L*=20/20, 20/1.2, 20/0.8, and 20/0.7 have been designed. The I_{DS} - V_{GS} and I_{DS}-V_{GS} characteristics at the temperature of 27, 55, 85, and 125 °C are measured. The threshold voltage was performing by the linear extrapolation methodology. The electrical characteristics such as threshold voltage, mobility, off-state leakage current, saturation current, and parasitic series *S/D* resistance are extracted and discussed. Finally, the temperature modeling parameters in BSIM3 level are proposed also.

Keywords: temperature dependence model, NMOSFET, threshold voltage, parasitic series resistance

1. Introduction

The operating temperature of the semiconductor devices affects the electrical characteristics and the circuit performance. There are two operating ranges concerned for the VLSI. They are the military (-55 °C to +125 °C) and the consumer-industrial (-25 °C to +85 °C) [1]. The temperature dependence parameter model is important for predicting the operation of devices and circuits. The *I-V* electrical characteristics of MOSFETs normally are strongly dependent on the operating temperature. The temperature parameter model of MOSFET should be known such as threshold voltage model, mobility model, and the parasitic series *S/D* resistance model. The temperature dependence model of the threshold voltage is defined as [2].

$$V_{TH}(T) = V_{TH}(T_{REF}) + \left[KT1 + \frac{KT1L}{L_{eff}} + KT2 \cdot V_{BS}\right]\left(\frac{T}{T_{REF}} - 1\right) \quad (1)$$

Where $V_{TH}(T_{REF})$ is the threshold voltage at a specific at T_{REF}. *KT1* is the temperature effect on the threshold voltage. *KT1L* is the channel length dependence of temperature sensitivity. *KT2* is the temperature effect on substrate bias on the threshold voltage. T_{REF} is the reference temperature. The subthreshold current (I_{sub}) is the current flow between the drain and source that occurs in a MOS transistor when the gate voltage is below V_{TH}. The subthreshold leakage current (BSIM) can be modeled as [2-4].

$$I_{sub} = I_o \, exp\left(\frac{V_{GS}-V_{TH}}{n(v_T)}\right)\left(1 - exp\left(\frac{-V_{DS}}{v_T}\right)\right) \quad (2)$$

$$I_o = \mu_o C_{ox} \frac{W_{eff}}{L_{eff}} (v_T)^2 \, exp(1.8) \quad (3)$$

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Where C_{ox} is the gate oxide capacitance per unit area, W_{eff} and L_{eff} are effective channel width and effective channel length, $v_T = kT/q$ is the thermal voltage. k is the Boltzmann constant. q is the electron charge. n is the subthreshold swing coefficient ($n = 1+C_D/C_{ox}$).

The off-state leakage current (I_{off}) is defined by the subthreshold current at 0V of V_{GS} and 5V of V_{DS}. The term $(1 - exp(-V_{DS}/v_T)$ can be neglected. The off-state leakage current at zero substrate bias can be described as following.

$$I_{off} = I_o \, exp\left(\frac{-V_{TH}+\eta V_{DS}}{n(v_T)}\right) \tag{4}$$

The threshold slope ($S = (ln\,10)nv_T$) of the transistor gives the inverse of the slope of I_{DS} versus V_{GS} in mV/dec of change in I_{DS}. The ideal of S at room temperature is 60 mV/dec. The drain current model is simplified as [2-7].

$$I_{DS}(T) = K_P(T)\frac{W_{eff}}{L_{eff}}\left[(V_{GS} - V_{TH}(T)) - \frac{V_{DS}}{2}\right]V_{DS} \tag{5}$$

$$K_P = \mu_{eff} C_{ox} \tag{6}$$

$$\mu_{eff} = \frac{U_o}{1+\theta(V_{GS}-V_{TH})} \tag{7}$$

$$K_P(T) = K_P(T_{REF})\left(\frac{T}{T_{REF}}\right)^{UTE} \tag{8}$$

Where K_P is the process transconductance. U_0 is low field mobility on operating temperature. UTE is the temperature effect on the low drain bias mobility. μ_{eff} is effective mobility. θ is the mobility degradation. The S/D series resistance is weakly influenced by changes in temperature [2]. In BSIM 3 model, the temperature dependence of the parasitic series S/D resistance is described by

$$R_{DSW}(T) = RDSW + PRT\left(\frac{T}{T_{REF}} - 1\right) \tag{9}$$

Where $RDSW$ is the S/D series resistance per unit width (Ω-μm) extracted at $T=T_{REF}$. PRT is the temperature coefficient for $RDSW$.

2. Materials and Methods

The devices in this paper were fabricated by sub-micrometer CMOS technology fabrication (TMCN-08) at the Thai Micro Electronics Center (TMEC). Starting with p-type substrate resistance of 25 Ω-cm, the N-Well was formed by the phosphorus implantation process with a dosage of 7×10^{12} cm^{-2} and with energy at 140 keV, resulting in a doping concentration of 6×10^{16} cm^{-3}. The p-well doping concentration of 5×10^{16} cm^{-3} was formed for the APT process. A self-aligns n+ polysilicon gate process 350 nm of thickness was used with gate oxide 15 nm of thickness. BF_2^+ ion implantation with a dosage of 1×10^{12} cm^{-2} and 70 keV of energy for threshold voltage adjustment process in a channel was implemented in order to match the threshold voltage of the NMOS and PMOS device as required in the modern CMOS technology process. The D/S doping concentration is approximately 1×10^{20} cm^{-3}. The D/S sheet resistance of NMOS is approximately 50 Ω/Sq. The D/S junction depth is

approximately 0.4 μm. The scalable device test structure has been designed for different device geometries: Big dimension (W=20 μm, L=20 μm) and short dimension (L=0.6 μm, 0.7 μm 0.8 μm, 1.2 μm, W=20 μm). The testing system is a precision semiconductor parameter analyzer Agilent B-1500A model, the wafer probing cascade Microtech M150 model with a thermal chuck in the range of 25 °C to 200 °C in manual operation. The measurement method is performed by setting reverse substrate bias V_{BS}=0 V, V_{DS}=0.1 V for the linear region and V_{DS} =5.0 V for saturation region measurement respectively. The Gate-Source voltage (V_{GS}) is swept from 0 to 5.0 V with 50 mV per step.

3. Results and discussion

The I_{DS}-V_{GS} of NMOS with V_{GS} was swept from 0 to 5.0 V in the linear region (V_{DS}=0.1V) at zero substrate bias (V_{BS}=0) over the temperature in the range of 27, 55, 85, and 125 °C are shown in Fig. 1. The extracted threshold voltage by the linear extrapolation method [8-9] is 0.7, 0.67, 0.63, and 0.58 V over the temperature in the range of 27, 55, 85, and 125 °C respectively. The calculated process transconductance is approximately 98.5 μA/V^2, 85 μA/V^2, 73 μA/V^2, and 60 μA/V^2. Fig. 2 shows the I_{DS}-V_{GS} characteristics of NMOS at zero substrate bias in the subthreshold region (V_{DS}=0.1 V) over the temperature. The results show that the threshold voltage is decreased as the temperature increased. The lowering of the threshold voltage is accompanied by an increase of the drain current in the subthreshold region. The *ZTC* (Zero Temperature Coefficient) is the point that the drain current with a small temperature coefficient or the point that the drain current is almost not dependent on the temperature. The V_{GS} at the *ZTC* point is about 0.95 V of NMOS (W/L=20/20). As seen that the drain current increases when the mobility increases, and the threshold voltage decreases. The mobility and threshold voltage both decrease, and the series resistance increase when the temperature increases. At any V_{GS} bias point, the three effects can cancel each other at a specific V_{GS} bias point. The threshold voltage versus the operating temperature is illustrated in Fig. 3. The V_{TH} of MOS with W/L=20/20 and W/L=20/1.2 are almost the same value since these devices are in the big dimension.

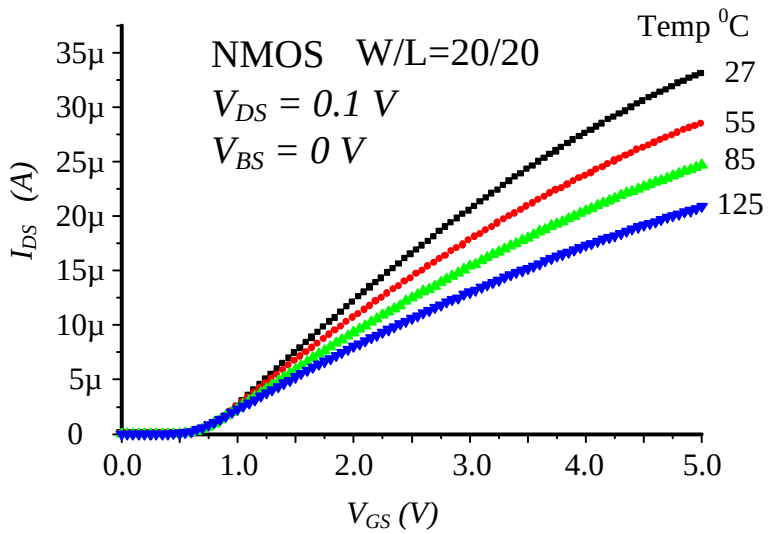

Fig. 1. I_{DS} - V_{GS} of NMOS at various temperature

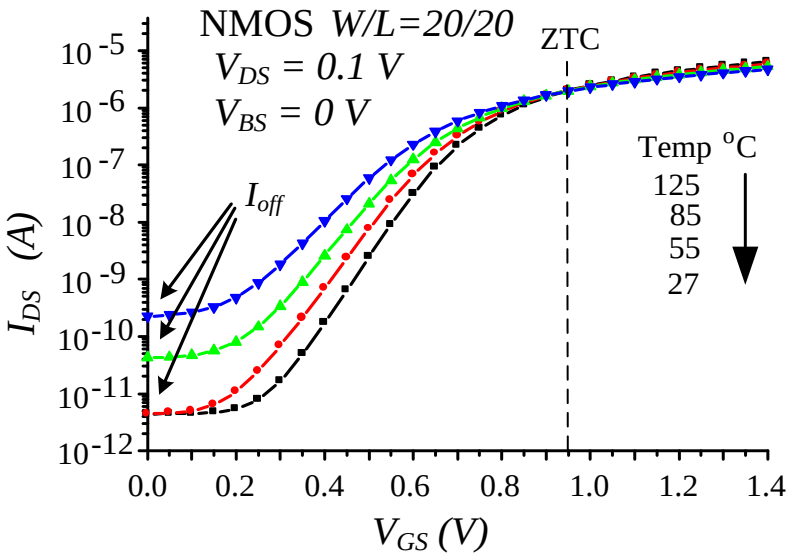

Fig. 2. I_{DS} - V_{GS} of NMOS in subthreshold region at various temperature

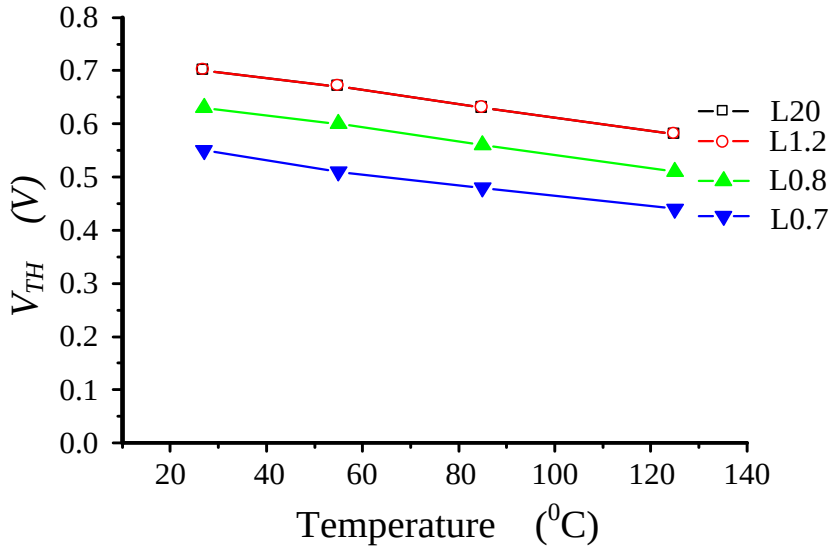

Fig. 3. V_{TH} versus temperature of NMOS at various channel length L=20, 1.2, 0.8 and 0.7 μm

Fig. 4 shows the threshold voltage versus channel length with an operating temperature as a parameter. The threshold voltage decreases rapidly for the channel length (Lg) lower than 0.7 μm for all operating temperature. The device transconductance (K_PW/L) versus temperature is illustrated in Fig. 5.

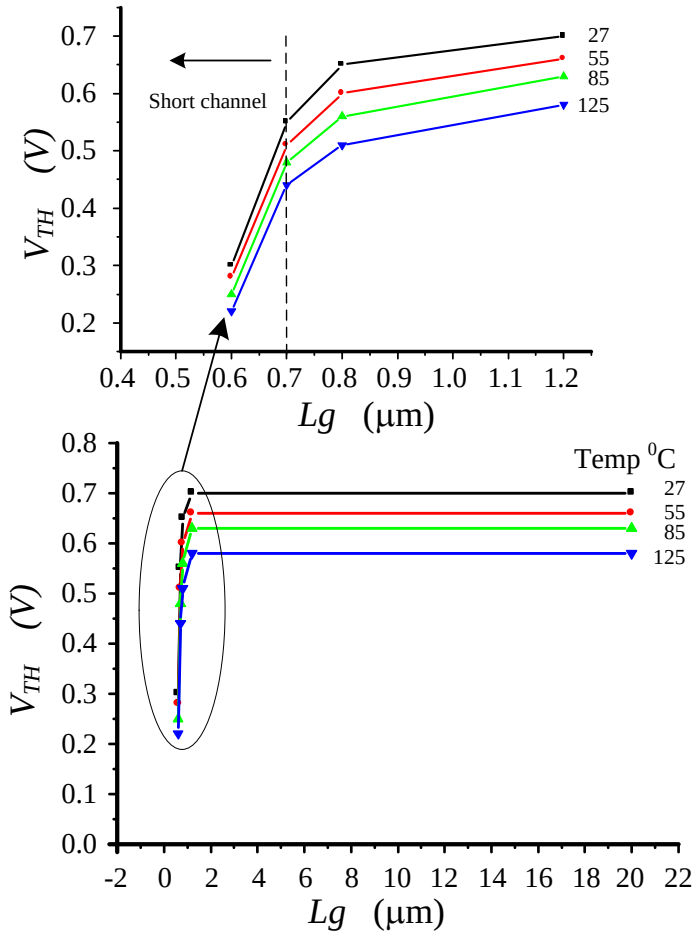

Fig. 4. V_{TH} versus L_g with various temperature for the test NMOS devices of W=20 μm

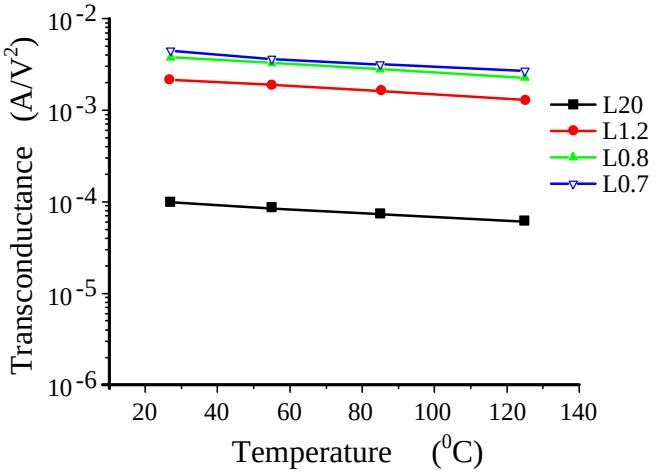

Fig. 5. Device transconductance versus temperature of NMOS at various channel lengths.

As seen that the device's transconductance is decreased approximately by the factor of 60% for all the channel length. The transconductance model over the operating temperature can be defined as

$$K_P(T) = 98.5 \times 10^{-6} \left(\frac{T}{T_{REF}}\right)^{-1.7} \quad (10)$$

In the same way, the mobility model can be defined as

$$U_0(T) = 454 \left(\frac{T}{T_{REF}}\right)^{-1.7} \quad (11)$$

Fig. 6 shows that at the reference temperature (T_{REF}), at Lg=1.2 and 0.8 μm. The off-state leakage current is approximately in the order 10^{-12}-10^{-11} A. The leakage current is increased by power 10^3 over the temperature 27 °C to 125 °C. For Lg=0.7 μm, the NMOS is in the short channel devices. At the reference temperature (T_{REF}), the threshold voltage is decreased rapidly then the off-state leakage current is increased rapidly also. The off-state leakage current is in the order of 10^{-6} A and does not change rapidly with the temperature. In short channel devices, the accuracy of mobility and threshold voltage model should be calculated. The *RDSW* versus the temperature is shown in Fig. 7.

The mobility is depended on the impurity concentration, defect concentration, temperature, and electron and hole concentrations and is also depended on the electric field, particularly at high fields. Like the carrier mobility, the series resistance is depended on the temperature and mobility by the relation ($R \propto 1/(nq\mu)$). In BSIM3, the temperature dependence on the *S/D* series resistance is described by (9). The parasitic resistance per unit width of Source/Drain *RDSW* [8] has a positive temperature coefficient. The results show that the *PRT* is about 0.7 ohm-μm. The temperature modeling parameters are listed in table 1.

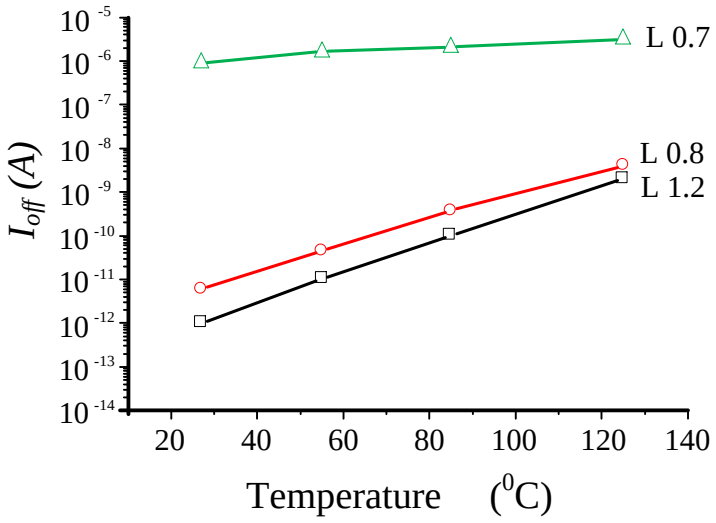

Fig. 6. I_{off} versus temperature of NMOS at various channel length L=1.2, 0.8, and 0.7 μm.

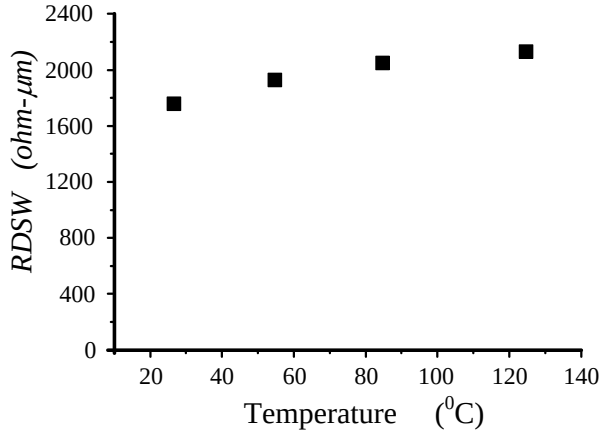

Fig. 7. *RDSW* versus temperature of NMOS

Table.1 Temperature Modeling Parameters

Parameter Description	Symbol	Value	Unit
Reference temperature at which parameter are extracted	T_{REF}	300	K
Temperature coefficient for threshold voltage	*KT1*	-0.38	V
Channel length sensitivity of temperature coefficient for threshold voltage	*KT1L*	0.0	Vm
Body bias coefficient of threshold voltage temperature effect	*KT2*	2.4×10^{-2}	
Temperature effect on low field mobility	*UTE*	-1.7	
Temperature-dependent on RDSW	*PRT*	0.7	ohm-μm

4. Conclusion

The temperature dependence model parameters on NMOSFET are investigated. The different sizes of testing devices with various structural *W/L*=20/20, 20/1.2, 20/0.8, and 20/0.7 have been designed. The I_{DS}-V_{GS} and I_{DS}-V_{GS} characteristics curve at various temperatures are measured. The threshold voltage was performing by the linear extrapolation methodology. The results show that parameter V_{TH}, K_P, *Uo*, and $I_{DS,Sat}$ is decreased as the temperature increases. On the other hand, the parameter I_{off} and series *S/D* resistance are increased. The leakage current I_{off} is in the order 10^{-12}-10^{-11} A and the leakage current I_{off} is increased by power 10^3 over the temperature 27 °C to 125 °C. For *Lg*=0.7 μm, the NMOS is in the short channel devices. The I_{off} is in the order of 10^{-6} A and does not change rapidly with the temperature. The model parameter of short channel devices should be extracted accurately. The parameter *PRT* is increased about 0.7 ohm-μm over the temperature range 27 °C to 125 °C. The temperature modeling parameters in BSIM3 level are proposed also.

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